UNIVERSAL PFC CONTROLLER

Firmware Reference Manual

Revision	Date	Firmware Version	Author	Description
01	02-17-2026	release-v1.0.0	Behjati H.	

Contents

1 Introduction

This document constitutes the Firmware Reference Manual for a Universal PFC Controller.

The presented PFC controller is universal because it supports various permutations of Control Method[1], PFC Type[2], and Control Mode[3], as seen in the Table 1 below.

Table 1: Various permutations of Control Method, PFC Type, and Control Mode.

Control Method[1]	PFC Type[2]	Control Mode[3]
ACC	Single Phase Mains - Totem Pole	Voltage Control
ACC	Single Phase Mains - Totem Pole	Power Control
ACC	Single Phase Mains - Passive Bridge	Voltage Control
ACC	Single Phase Mains - Passive Bridge	Power Control
RFC	Single Phase Mains - Totem Pole	Voltage Control
RFC	Single Phase Mains - Totem Pole	Power Control
RFC	Three Phase Mains - Six Switch	Voltage Control
RFC	Three Phase Mains - Six Switch	Power Control

Acronym	Expansion
ACC	Average Current Control
RFC	Reference Frame Control

- **Control Method[1]** is set up as a build configuration to save flash space and execution time, i.e. only the code belonging to the selected control method is compiled (in addition to the common code). It is selected by the preprocessor definitions `CTRL_METHOD_ACC` or `CTRL_METHOD_RFC`.
- **PFC Type[2]** is selected via the parameter `params.pfc.nom.type`.
- **Control Mode[3]** is selected via the parameter `params.ctrl.id.mode`.
- ***N-Phase Interleaving** is supported for all permutations of control modes and is selected via the parameters `NOIP` (Number of Interleaved Phases), and `NOIC` (Number of Independent Current Loops).

The presented PFC Controller is hardware agnostic and can work across multiple hardware platforms with different microcontroller families and power boards.

The remaining chapters of this document present the details of the nested control loops in ACC / RFC, state machine, system identification algorithm, and parameters dictionary.

The last chapter (parameters dictionary) provides a one-to-one mapping between the materials provided in this document and their corresponding parameters in the firmware.

2 Average Current Control (ACC)

In ACC, the *"shape"* of the input current i_g is controlled to be the same as the shape of the grid voltage e_g, whereas the *"magnitude"* of the input current i_g is controlled such that there is enough input power P_{in} to sustain the output voltage v_{out} at a regulated level V_{out}^*.

Therefore, if the shape of grid voltage e_g is sinusoidal, the shape of input current i_g will also be sinusoidal with the same phase and the power factor will be 1.0.

2.1 Single-Phase-Mains Totem-Pole PFC (1ϕ-TP-PFC)

Figure 1 depicts the general topology of a 1ϕ-TP-PFC.

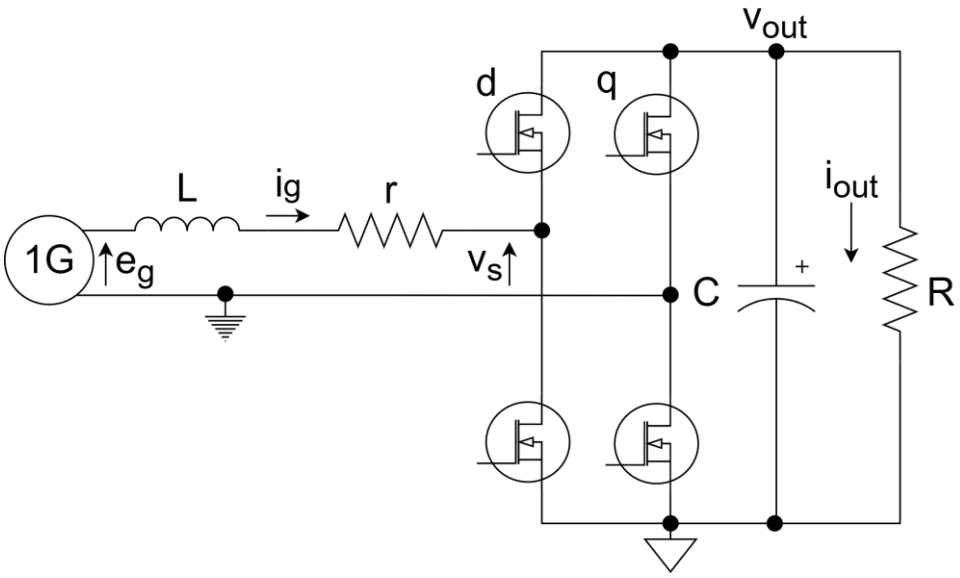

Figure 1: 1ϕ-TP-PFC type

The high-frequency switching leg is controlled by applying a certain PWM frequency f_s and duty cycle d, whereas the low-frequency switching leg is controlled by a switching command $q \epsilon \{0,1\}$ that changes every half of the mains cycle T_g.

Both d and q correspond to the upper switches in the switching legs. The lower switches will have complementary duty cycle and switching command, i.e. $(1-d)$ and $\overline{q}$, respectively.

2.1.1 Current Loop

Here, we will denote the average of a variable x over a switching cycle T_s as

$$\langle x \rangle_{T_s} = \langle x \rangle \quad (1)$$

From Figure 1, the input current (i_g) dynamics can be expressed as

$$L\frac{d\langle i_g \rangle}{dt} + r\langle i_g \rangle = \langle e_g \rangle - \langle v_s \rangle \quad (2)$$

For simplicity, we will drop the average sign $\langle \cdot \rangle$ here but all variables denote their corresponding averages over a switching cycle T_s:

$$L\frac{di_g}{dt} + ri_g = e_g - v_s \quad (3)$$

For current regulation, a model of the plant based on (3) can be constructed as seen in Figure 2.

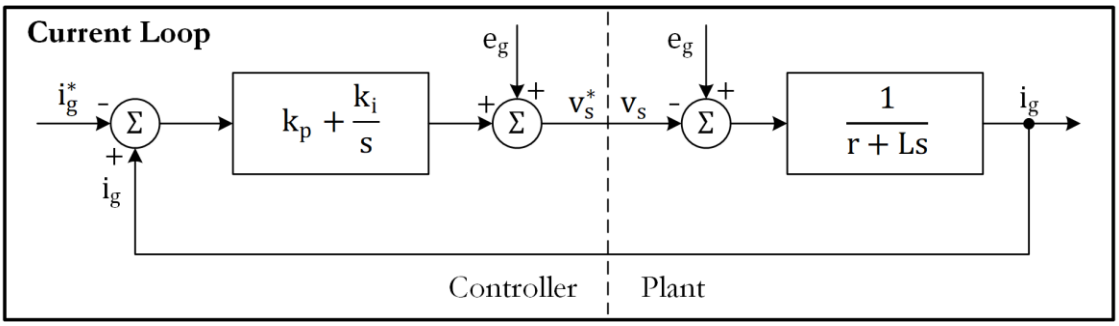

Figure 2: Current loop: 1ϕ PFC in ACC

As seen in Figure 2, a feed forward term e_g is added to the PI regulator's output on the controller side to eliminate the effect of e_g on the plant side and improve the dynamic response of the system.

Based on Figure 2, it can be shown that the following choices of k_p and k_i will result in a first-order damped system with the desired cross over frequency (i.e. bandwidth) of ω_c:

$$\begin{cases} k_p = L\omega_c \\ k_i = r\omega_c \end{cases} \quad (4)$$

Hence, k_p and k_i can be auto-calculated by the firmware based on the desired cross over frequency of the current controller ω_c and circuit parameters r and L.

2.1.2 Voltage Loop

The voltage loop must maintain a power balance between the power demanded by the load and power provided by the converter. If the power balance is maintained, the output voltage will stay regulated.

Figure 3 depicts the block diagram of the voltage loop, including the controller and plant.

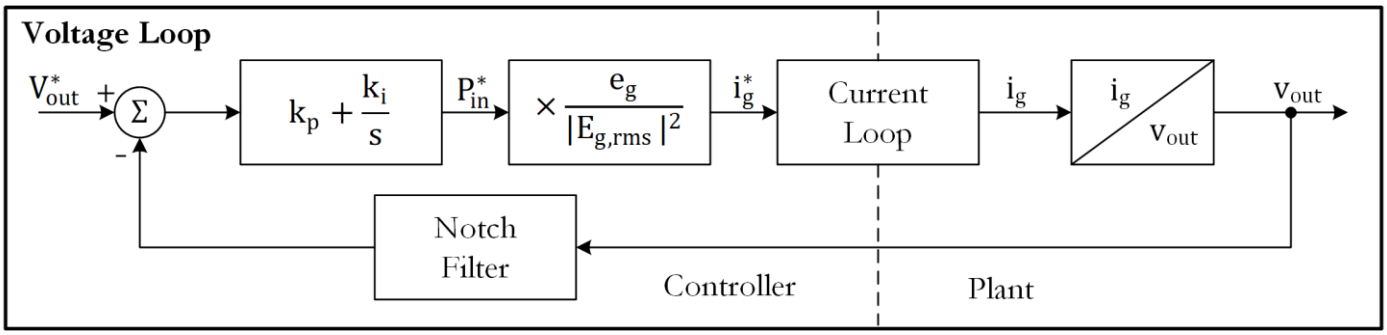

Figure 3: Voltage loop: 1ϕ PFC in ACC

The input to the current loop, as depicted in Figure 2, is the current command i_g^*. The multiplication block, $e_g/|E_{g,rms}|^2$ in Figure 3 ensures that the current command's shape i_g^* is the same as the grid voltage's shape e_g. In order to prove that the output of the PI regulator block is indeed the command input power P_{in}^*, we can express the PI regulator's output as

$$i_g^* \Big/ \left(\frac{e_g}{|E_{g,rms}|^2} \right) = \frac{|E_{g,rms}|^2}{(e_g/i_g^*)} = \frac{|E_{g,rms}|^2}{R_e} = P_{in}^* \quad (5)$$

where R_e is the effective input resistance defined as

$$\frac{e_g}{i_g} = R_e \quad (6)$$

The output power can be written based on the input power as

$$P_{out} = \eta P_{in} \quad (7)$$

The output power can also be written in terms of the power demand by the load as

$$P_{out} = v_{out}\left(i_{out} + C\frac{dv_{out}}{dt}\right) \quad (8)$$

Applying small-signal perturbations on (8) and linearizing the result around the quiescent point would yield

$$\hat{P}_{out} = V_{out}\left(\hat{\imath}_{out} + C\frac{d\hat{v}_{out}}{dt}\right) + \hat{v}_{out}\underbrace{I_{out}}_{V_{out}/R} \quad (9)$$

where $\hat{x}$ and X denote the small-signal perturbation and steady-state values of x, respectively.

Thus, (9) can be rewritten as

$$\hat{P}_{out} = V_{out}\left(\frac{\hat{v}_{out}}{R} + C\frac{d\hat{v}_{out}}{dt}\right) + V_{out}\hat{\imath}_{out} \quad (10)$$

i.e.

$$\hat{P}_{out} = V_{out}\left(\left(\frac{1+RCs}{R}\right)\hat{v}_{out} + \hat{\imath}_{out}\right) \quad (11)$$

From (7) and (11), the transfer function of the plant from input power $\hat{P}_{in}$ to output voltage $\hat{v}_{out}$ can be expressed as

$$\hat{v}_{out} = \left(\frac{R}{1+RCs}\right)\left(\frac{\eta\hat{P}_{in}}{V_{out}} - \hat{\imath}_{out}\right) \quad (12)$$

Figure 4 illustrates the equivalent model of the voltage loop (Figure 3) based on the power balance principle set forth in (12).

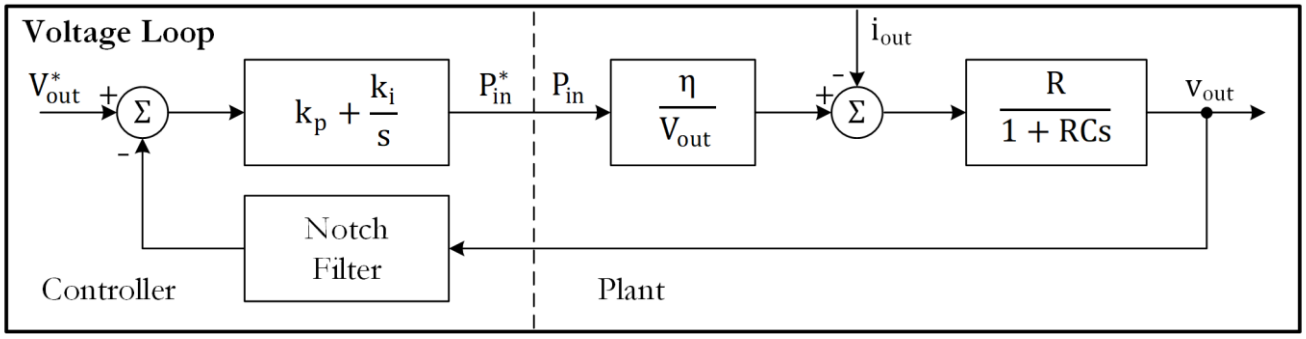

Figure 4: Equivalent voltage loop: 1ϕ PFC in ACC

As seen in Figure 4, the output current transients $\hat{\imath}_{out}$ is a disturbance that can be damped by the controller. The PI regulator coefficients k_p and k_i can be auto-calculated by the firmware based on the desired corner frequency ω_c (i.e. bandwidth) and the circuit parameters R and C as

$$\begin{cases} k_p = (RC\omega_c)(V_{out}/R) = (V_{out}\omega_c)\cdot C \\ k_i = (\omega_c)(V_{out}/R) = (V_{out}\omega_c)/R \end{cases} \quad (13)$$

2.1.3 Voltage Modulator

The objective of the voltage modulator is to apply the necessary duty cycle d and switching command q for the high-frequency and low-frequency legs such that the desired switching voltage v_s is realized.

The switching voltage v_s, duty cycle d, and switching command q can be derived as follows:

$$\begin{cases} v_s = (d-q)v_{out} \rightarrow \\ d = q + \dfrac{v_s}{v_{out}} \\ q = (v_s > 0)?\,0:1 \end{cases} \qquad (14)$$

$$\begin{cases} q \in \{0,1\} \\ 0 \le d \le 1 \\ -1 \le (d-q) \le 1 \\ -v_{out} \le v_s \le v_{out} \\ -E_g \le e_g \le E_g \end{cases}$$

The modulation scheme set forth in (14) will ensure that both positive and negative switching voltages v_s can be realized while the duty cycle d is strictly positive. This is done by proper modulation of the switching command q for the low-frequency leg as seen in (14).

Figure 5 depicts the voltage modulator for the 1ϕ-TP-PFC in ACC.

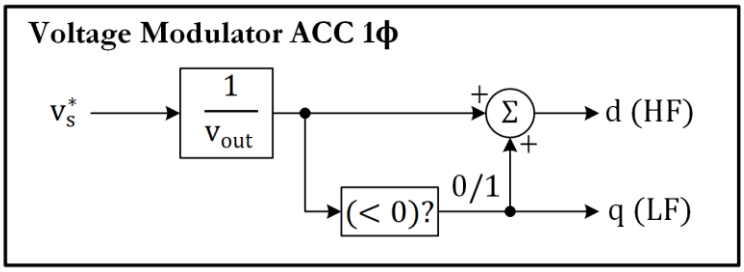

Figure 5: Voltage modulator: 1ϕ-TP-PFC in ACC

2.2 Single-Phase-Mains Passive-Bridge PFC (1ϕ-PB-PFC)

Figure 6 depicts the general topology of a 1ϕ-PB-PFC.

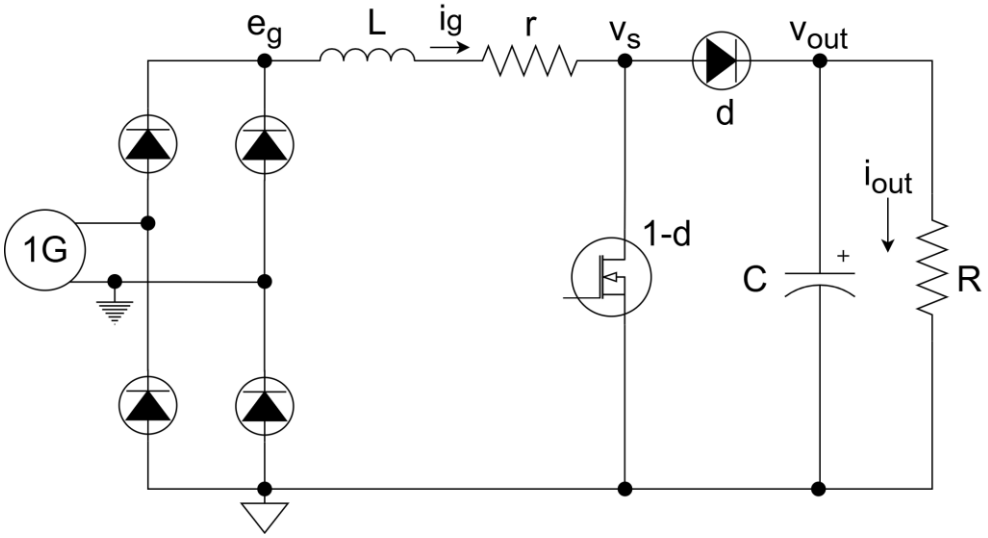

Figure 6: 1ϕ-PB-PFC Type

As opposed to the 1ϕ-TP-PFC shown in Figure 1, the 1ϕ-PB-PFC only has one active switch which makes its control simpler. However, since it has more switch / diode voltage drops in the path of the input current, it has a lower efficiency compared to 1ϕ-TP-PFC. Another disadvantage of the 1ϕ-PB-PFC seen in Figure 6 is that it can only support unidirectional power flow (from the grid to the load) whereas the 1ϕ-TP-PFC seen Figure 1 in can support bidirectional power flow, which is helpful in applications where energy needs to be pumped back to the grid (e.g. when the load is a motor driver inverter in regenerative breaking mode).

2.2.1 Current Loop

The current loop block diagram of 1ϕ-PB-PFC is identical to that of the 1ϕ-TP-PFC seen in Figure 2. However, current command i_{g}^{*} and current feedback i_{g} are all rectified sine waves as opposed to normal bidirectional sine waves i.e.

$$\begin{cases} i_{\mathrm{g}} = I_{\mathrm{g}}|\cos(\theta)| \\ i_{\mathrm{g}}^{*} = I_{\mathrm{g}}^{*}|\cos(\theta)| \end{cases} \quad (15)$$

Because all of the voltage and current waveforms are rectified sine waves, only ACC can be used to control this PFC type.

2.2.2 Voltage Loop

Similarly, the voltage block diagram of the 1ϕ-PB-PFC is identical to that of the 1ϕ-TP-PFC seen Figure 3 and Figure 4. However, the gird voltage e_{g} waveform is a rectified sine wave as opposed to a normal bidirectional sine wave:

$$e_{\mathrm{g}} = E_{\mathrm{g}}|\cos(\theta)| \quad (16)$$

2.2.3 Voltage Modulator

In 1ϕ-PB-PFC the switching voltage v_{s} cannot be negative (as opposed to 1ϕ-TP-PFC). On the other hand, there is only one degree of freedom in assigning the duty cycle d since there is no low-frequency switching leg q. It can be shown that the required duty cycle d to realize v_{s} would be calculated similar to (14) assuming that $q = 0$ i.e.

$$\begin{cases} v_{\mathrm{s}} = d v_{\mathrm{out}} \rightarrow \\ d = \dfrac{v_{\mathrm{s}}}{v_{\mathrm{out}}} \end{cases} \quad (17)$$

$$\begin{cases} 0 \le d \le 1 \\ 0 \le v_{\mathrm{s}} \le v_{\mathrm{out}} \\ 0 \le e_{\mathrm{g}} \le E_{\mathrm{g}} \end{cases}$$

3 Reference Frame Control (RFC)

In Reference Frame Control, the quadrature and direct components of the input currents are independently controlled. It can be shown that, in a synchronous reference frame where the grid voltage is completely aligned with the q axis, the real and reactive input power are directly proportional to the quadrature and direct components of the input currents, respectively.

Therefore, the reactive power can be controlled to be zero, thus realizing perfect power factor correction. In addition, the active power can be controlled to regulate the output voltage.

Since the quadrature and direct current components can be defined for both 1ϕ and 3ϕ, RFC can be used for controlling PFC converters with either single phase mains or three phase mains.

3.1 Three-Phase-Mains Six-Switch PFC (3ϕ-SS-PFC)

Figure 7 illustrates the topology of a general 3ϕ-SS-PFC.

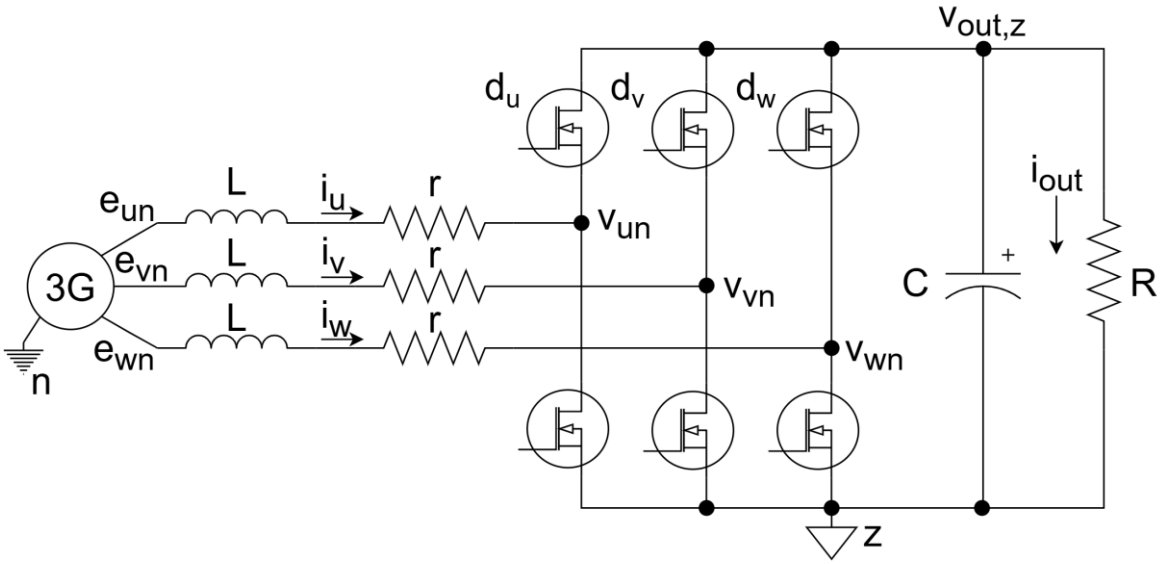

Figure 7: 3ϕ-SS-PFC type

It must be noted that the neutral point voltage of the grid (denoted by n) is not the same as the ground of the converter (denoted by z). However, with proper voltage modulation, v_{nz} can be controlled to be half of the output voltage $v_{\mathrm{out,z}}$. The switching and grid voltages, $\boldsymbol{v}_{\mathrm{uvw,n}}$ and $\boldsymbol{e}_{\mathrm{uvw,n}}$, are all referenced to the neutral point of the grid (n), whereas v_{out} is referenced to the ground of the converter (z). To simplify the equations, the subscripts n and z are removed hereafter.

3.1.1 Voltage Loop

Based on the circuit topology depicted in Figure 7, the input current dynamics as well as the input power can be expressed as

$$\begin{cases} L\dfrac{d\boldsymbol{i}_{\mathrm{uvw}}}{dt} + r\boldsymbol{i}_{\mathrm{uvw}} = \boldsymbol{e}_{\mathrm{uvw}} - \boldsymbol{v}_{\mathrm{uvw}} \\ P_{\mathrm{in}} = \boldsymbol{e}_{\mathrm{uvw}}^{T} \cdot \boldsymbol{i}_{\mathrm{uvw}} \end{cases} \tag{18}$$

Here, we will use the QD transform defined as

$$\boldsymbol{K}(\theta) = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta-\alpha) & \cos(\theta+\alpha) \\ \sin(\theta) & \sin(\theta-\alpha) & \sin(\theta+\alpha) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{19}$$

to transform all of the three-phase voltages and currents into a rotating reference frame with angle θ. The inverse QD transform can be written as

$$\boldsymbol{K}^{-1}(\theta)=\begin{bmatrix}\cos(\theta) & \sin(\theta) & 1\\ \cos(\theta-\alpha) & \sin(\theta-\alpha) & 1\\ \cos(\theta+\alpha) & \sin(\theta+\alpha) & 1\end{bmatrix} \quad (20)$$

Therefore, all variables can be transformed between three-phase and rotating reference frames based on:

$$\begin{cases}\boldsymbol{x}_{qd0}=\boldsymbol{K}(\theta)\boldsymbol{x}_{\mathrm{uvw}}\\ \boldsymbol{x}_{\mathrm{uvw}}=\boldsymbol{K}^{-1}(\theta)\boldsymbol{x}_{qd0}\end{cases} \quad (21)$$

The QD transform described in (19)-(21) can then be applied to (18) to transform it into a QD reference frame of an arbitrary angle θ:

$$\begin{cases}L\boldsymbol{K}\dfrac{d\left(\boldsymbol{K}^{-1}\boldsymbol{i}_{qd0}\right)}{dt}+r\boldsymbol{i}_{qd0}=\boldsymbol{e}_{qd0}-\boldsymbol{v}_{qd0}\\ P_{\mathrm{in}}=\boldsymbol{e}_{qd0}^{T}\cdot\boldsymbol{K}^{-T}\cdot\boldsymbol{K}^{-1}\boldsymbol{i}_{qd0}\end{cases} \quad (22)$$

Simplifying (22) would result in

$$\begin{cases}L\dfrac{di_q}{dt}+L\omega i_d+ri_q=e_q-v_q\\ L\dfrac{di_d}{dt}-L\omega i_q+ri_d=e_d-v_d\\ P_{\mathrm{in}}=\dfrac{3}{2}\left(e_qi_q+e_di_d\right)\\ Q_{\mathrm{in}}=\dfrac{3}{2}\left(e_qi_d-e_di_q\right)\end{cases} \quad (23)$$

The significance of (23) is that it shows by choosing the rotating reference frame such that the grid voltage is completely aligned with the Q axis and controlling the D axis current to be zero i.e.

$$\begin{cases}e_d=0\rightarrow\theta=?\\ i_d^{*}=0\end{cases} \quad (24)$$

we can prove that real input power is directly controlled by the Q-axis current i_q and the reactive input power is zero (power factor correction) i.e.

$$\begin{cases}P_{\mathrm{in}}=\dfrac{3}{2}\left(e_qi_q\right)\\ i_q=\left(\dfrac{1}{3}\right)\left(\dfrac{2}{e_q}\right)P_{\mathrm{in}}\\ Q_{\mathrm{in}}=0\rightarrow\mathrm{PF}=1\end{cases} \quad (25)$$

Similarly, for a PFC converter with 1ϕ mains, the same conclusion can be made except that there is a factor of 3 difference in the input active and reactive powers i.e.

$$\begin{cases}P_{\mathrm{in}}=\dfrac{1}{2}\left(e_qi_q\right)\\ i_q=\left(\dfrac{2}{e_q}\right)P_{\mathrm{in}}\end{cases} \quad (26)$$

We can even extend (25) and (26) to ACC as well to obtain a unified voltage controller that will work for all permutations of 1ϕ / 3ϕ and RFC / ACC. For ACC we can express the real input power as

$$\begin{cases}P_{\mathrm{in}}=E_{\mathrm{g,rms}}\cdot I_{\mathrm{g,rms}}=\dfrac{1}{2}\left(E_{\mathrm{g}}I_{\mathrm{g}}\right)\\ I_{\mathrm{g}}=\left(\dfrac{2}{E_{\mathrm{g}}}\right)P_{\mathrm{in}}\end{cases} \quad (27)$$

Combining (25)-(27), we can obtain a unified voltage loop that will work for all of the mentioned permutations as seen in Figure 8 below:

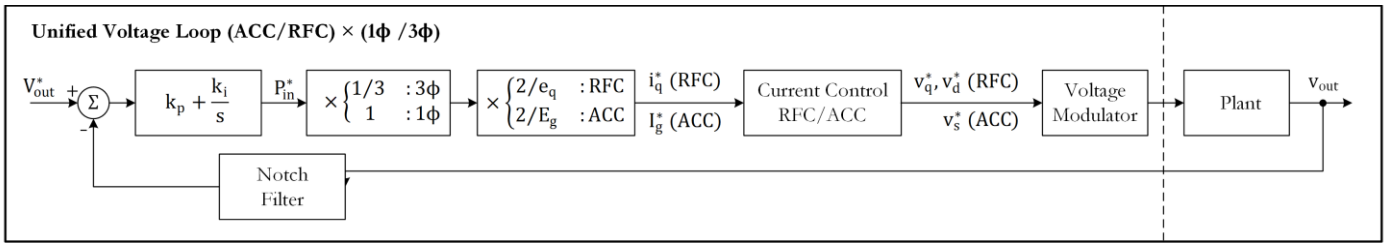

Figure 8: Unified voltage loop: 1ϕ & 3ϕ in ACC & RFC

3.1.2 Current Loop

Figure 9 depicts the block diagram of the quadrature and direct current loops in RFC. As seen in (24)-(26), the current command for the direct axis i_d^* must be set to zero to achieve power factor correction. It must be noted that RFC allows for nonzero i_d^* as well, which can be beneficial in certain applications for reactive power generation to compensate for other reactive loads nearby.

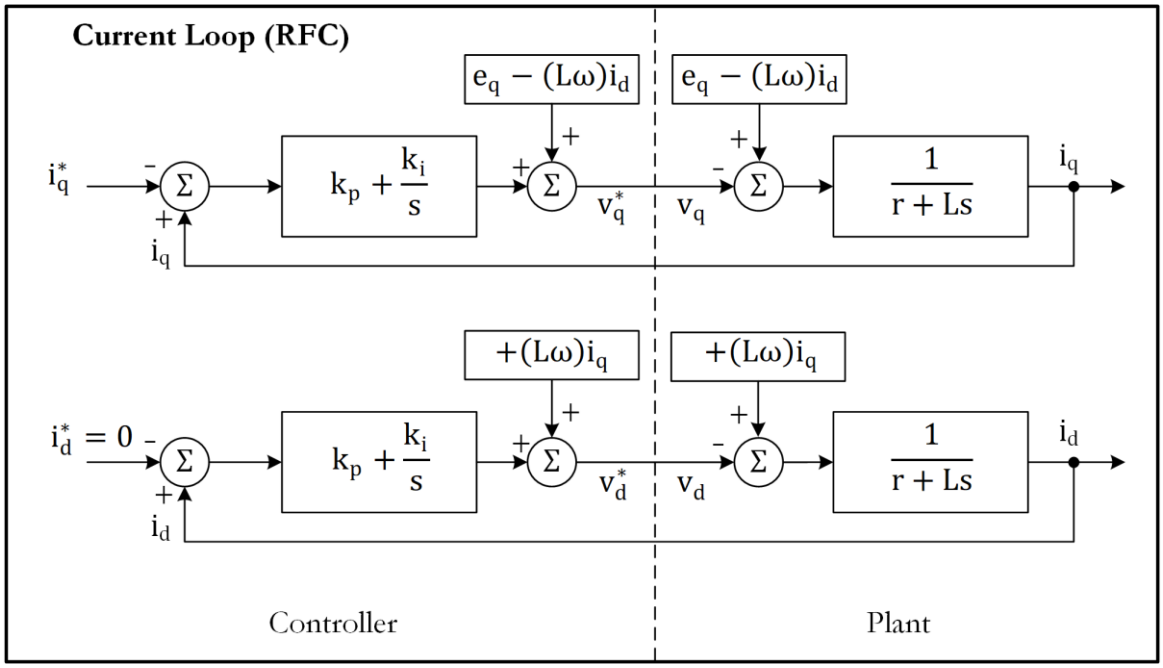

Figure 9: Current loops: 1ϕ & 3ϕ in RFC

The feed forward terms in Figure 9, which are added to the outputs of the PI regulators on the controller side, decouple the Q- and D-axis controllers. In addition, the feedforward terms shift the steady-state output of the PI regulators to zero, hence the PI regulators only compensate the disturbances and feed-forward model inaccuracies. Overall, the feedforward terms improve the dynamic performance of the current controllers.

3.1.3 Voltage Modulator

Figure 10 illustrates the block diagram of the voltage modulator for 3ϕ-SS-PFC in RFC. It must be noted that the maximum value for command phase voltages $\boldsymbol{v}_{\mathrm{uvw}}^*$ is half of v_{out}. In addition, the 0.5 offset in the modulation scheme seen in Figure 10 ensures that v_{nz} is controlled to be half of the output voltage $v_{\mathrm{out,z}}$, as described in section 3.1.

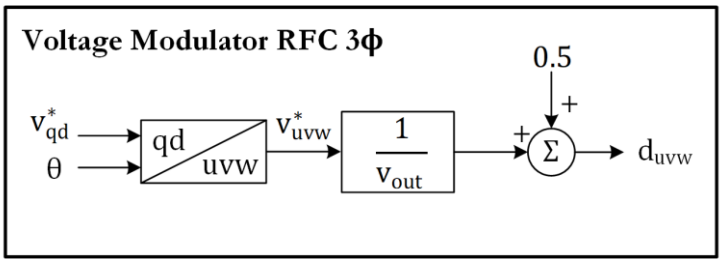

Figure 10: Voltage modulator: 3ϕ-SS-PFC in RFC

3.1.4 Phase Lock Loop (PLL)

As explained in (24), the chosen reference frame must be synchronized with the grid voltage such that the grid voltage is always aligned with the Q-axis i.e. $e_d = 0$. In order to synchronize the reference frame with the grid voltage such that $e_d = 0$, a PLL is required as shown below.

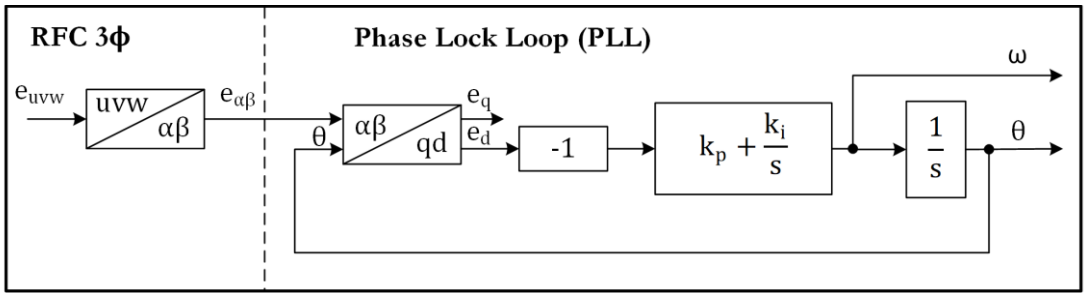

Figure 11: PLL: 3ϕ PFC in RFC

The PLL is inherently a nonlinear loop due to sine and cosine terms in the QD transform block. However, it can be shown that the small-signal loop gain $G(s)$ can be approximated as a Linear-Time-Invariant (LTI) system as

$$G(s) = A\left(k_p + \frac{k_i}{s}\right)\frac{1}{s} \quad (28)$$

Thus, the small-signal closed-loop transfer function would be

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{Ak_p s + Ak_i}{s^2 + Ak_p s + Ak_i} \quad (29)$$

From (29), the firmware can auto-calculate k_p and k_i coefficients based on the desired corner frequency ω_c (i.e. bandwidth) assuming an optimal damping factor of $\xi = \frac{1}{\sqrt{2}} = 0.707$:

$$\begin{cases} k_i = \dfrac{\omega_c^2}{A} \\ k_p = \dfrac{2\xi\omega_c}{A}\Big|_{\xi=\frac{1}{\sqrt{2}}} = \dfrac{\sqrt{2}\omega_c}{A} \end{cases} \quad (30)$$

3.2 Single-Phase-Mains Totem-Pole PFC (1ϕ-TP-PFC)

The 1ϕ-TP-PFC topology presented in Figure 1 can be also controlled in RFC mode, similar to a 3ϕ-SS-PFC presented in section 3.1.

3.2.1 Voltage Loop

The unified voltage control loop presented in Figure 8 will work seamlessly for 1ϕ-TP-PFC as well. The difference between 3ϕ and 1ϕ would only be the 1/3 multiplication factor applied on the output of the voltage PI regulator P_{in}^{*} as shown in Figure 8.

3.2.2 Current Loop

The quadrature and direct current loop regulators presented in Figure 9 will work seamlessly for 1ϕ-TP-PFC as well. There is no difference between 3ϕ and 1ϕ in regulating the quadrature and direct axis currents.

Here, we can extend the current loop controller in Figure 8 in order to seamlessly support ACC as well. Figure 12 depicts the block diagram of the current regulator in ACC, which would be identical to the current regulator presented earlier in Figure 2. However, the ACC current regulator in Figure 12 can be used together with the unified voltage controller in Figure 8 in order to obtain a unified PFC library that supports all of these permutations.

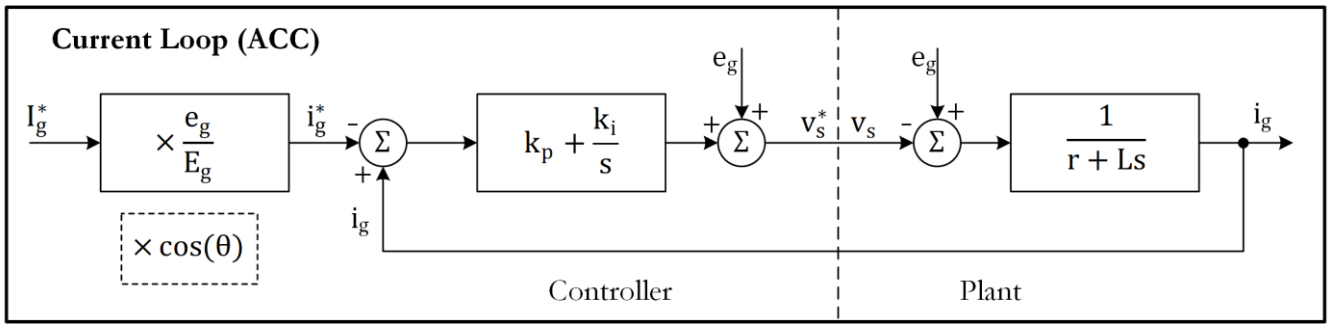

Figure 12: Equivalent current loop: 1ϕ PFC in ACC

3.2.3 Voltage Modulator

The voltage modulator of 1ϕ-TP-PFC in RFC would be similar to that in ACC (Figure 5) except that the switching voltage command v_s^* is synthesized from QD axes voltage commands in RFC as shown in Figure 13 below.

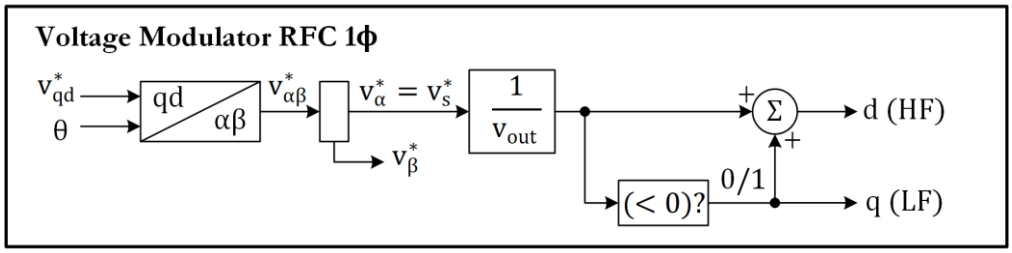

Figure 13: Voltage modulator: 1ϕ-TP-PFC in RFC

3.2.4 Second-Order Generalized Integrator (SOGI)

As opposed to 3ϕ-SS-PFC where there are three grid voltages, in 1ϕ-TP-PFC, there is a single grid voltage. Therefore, the quadrature and direct components of the grid voltage must be synthesized from a single grid voltage. The QD transform described in (19) only acts on 3ϕ variables. Therefore, the quadrature and direct components of the grid voltage must be synthesized in another way. Usually the stationary reference frame $\alpha\beta$ components of the grid voltage are synthesized first, and then Parke transform is used to obtain the qd components.

SOGI is one of the robust methods of synthesizing the stationary reference frame $\alpha\beta$ components. Figure 14 depicts the block diagram of a SOGI used to synthesize stationary frame grid voltages $\boldsymbol{e}'_{\alpha\beta}$ and the cascaded PLL for obtaining the reference frame angle θ and the grid frequency ω.

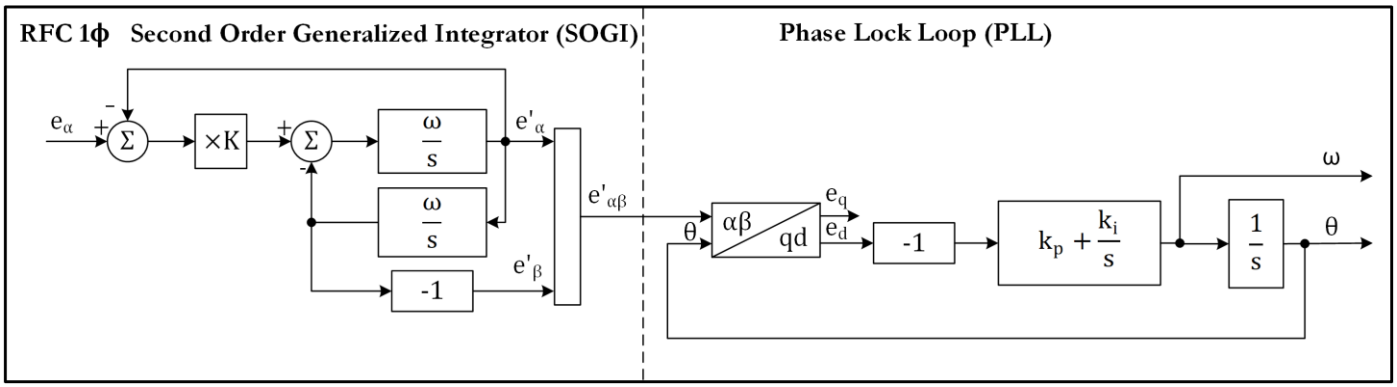

Figure 14:SOGI + PLL: 1ϕ-TP-PFC in RFC

From Figure 14, the transfer functions of the synthesized stationary frame grid voltages $\boldsymbol{e}'_{\alpha\beta}$ can be written in terms of the actual grid voltage e_α as

$$\begin{cases} \dfrac{e'_\alpha}{e_\alpha} = \dfrac{K\omega s}{s^2 + K\omega s + \omega^2}\Big|_{s=j\omega} = 1 \\ \dfrac{e'_\beta}{e_\alpha} = \dfrac{K\omega^2}{s^2 + K\omega s + \omega^2}\Big|_{s=j\omega} = e^{-j\frac{\pi}{2}} \end{cases} \quad (31)$$

The integrator gains of the SOGI in Figure 14 are adaptive and change as the estimated grid frequency ω changes, such that at the grid frequency $s = j\omega$, $e'_\alpha = e_\alpha$ and $e'_\beta = e^{-j\pi/2} e_\alpha$ i.e. the β component has a phase lag of exactly 90 degrees. This proves that the β component is correctly synthesized at the grid frequency ω.

3.2.5 Phase Lock Loop (PLL)

The PLL for 1ϕ-TP-PFC presented in Figure 14 is identical to that of the 3ϕ-SS-PFC. Therefore, it follows the same operational principles set forth in (28)-(30).

4 State Machine

Figure 15 illustrates the state machine diagram of the Universal PFC Controller.

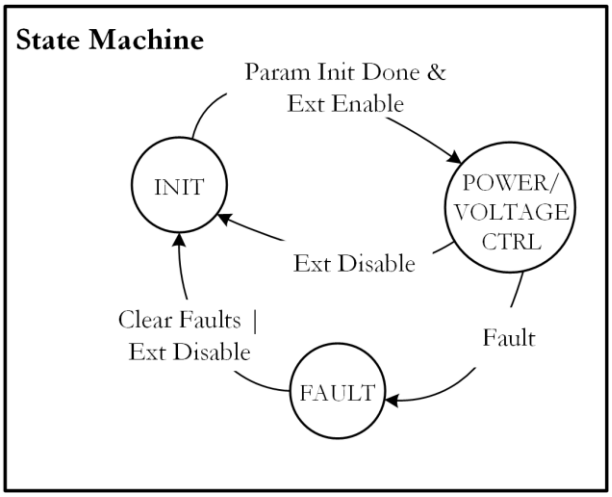

Figure 15: State machine diagram

The description of each state as well as the applicable control methods are listed in Table 2.

Table 2: States in the state machine.

State	Used in		Description
INIT	ACC	RFC	This is the first state by default where parameter initializations happen.
	✓	✓	
POWER CTRL	ACC	RFC	In this state, the input power is regulated. Power regulation is mostly used for testing purposes.
	✓	✓	
VOLTAGE CTRL	ACC	RFC	In this state, the output voltage is regulated.
	✓	✓	
FAULT	ACC	RFC	Fault state.
	✓	✓	

5 Parameters Dictionary

The following table presents a list of tunable parameters for various control methods ACC & RFC (which are selected as build configurations). The firmware symbol, as well as the parameter type, its SI unit, the corresponding section in this document, and the corresponding mathematical symbol in that section are listed. This table provides a one-to-one mapping between the materials provided in this document and their corresponding parameters in the firmware.

There are two parameter types, Basic and Advanced. Advanced parameters don't need to be entered by the user. They can be auto-calculated by the firmware by invoking the auto-calculate function through the debugger or the GUI. The user can also set the advanced parameters directly if fine tuning is required. Usually, auto-calculation results in close-to-optimal results for initial evaluation but the advanced parameters can be further fine-tuned directly if desired.

In addition, not all basic parameters need to be touched for the control system to work. Only a few basic parameters usually need to be touched to get the system up and running. The firmware is very flexible and versatile, and all of the parameters can be finely tuned but that doesn't mean that they must be changed for the system to work.

Table 3: Parameters dictionary

Build	FW Symbol	Type	Unit	Section	Symbol
ACC, RFC	TBD	B	-		
	…				